

3. A nonvolatile semiconductor memory device according to claim 1, further comprising a write driver and a sense amplifier.

4. A nonvolatile semiconductor memory device according to claim 3, wherein the write driver and sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation.

5. A sector structure of a nonvolatile semiconductor memory, said sector structure comprising:

a plurality of memory cell transistors arranged in a cell array block; and
a plurality of decoder transistors arranged in a column decoder block, wherein said memory cell transistors and decoder transistors are arranged on a common bulk region.

6. A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein an erase operation is configured to erase all of the transistors in the sector simultaneously.

7. A sector structure of a nonvolatile semiconductor memory according to claim 5, said sector structure further comprising:

a plurality of word lines arranged in the cell array block, each word line being connected to a plurality of cell gates;
a plurality of bit lines arranged in the cell array block, each bit line being connected to a plurality of memory cell drains;
a plurality of common data lines connected to the bit lines;
a plurality of write drivers, each connected to a respective one of the common data lines; and
a plurality of sense amplifiers, each connected to a respective one of the common data lines.

8. A sector structure of a nonvolatile semiconductor memory according to claim 7, wherein each write driver and sense amplifier is configured to be placed in a state of high impedance during an erase operation.

9. A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein said sector structure is configured to provide 64 Kbytes of memory.

10. A nonvolatile semiconductor memory device, comprising:
a cell array block comprising a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of a plurality of word lines, each drain being connected to a corresponding bit line out of a plurality of bit lines;
a source line driver commonly connected to sources of each memory cell transistor in the cell array block to apply a source voltage;
a plurality of sectors, each sector comprising transistors of a column decoder connected between a plurality of bit lines and common data lines to select one bit line out of the plurality of bit lines; and
a common bulk region arranged in each sector, wherein the memory cell transistors and the column decoder transistors of each sector share the common bulk region; and
a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

11. A nonvolatile semiconductor memory device according to claim 10, wherein the memory device is a NOR-type flash EEPROM.

12. A nonvolatile semiconductor memory device according to claim 10, wherein the bulk region is a pocket P-well.

13. A nonvolatile semiconductor memory device according to claim 10, further comprising a plurality of write drivers and sense amplifiers, wherein each data line is connected to a corresponding one of the write drivers and a corresponding one of the sense amplifiers.

14. A nonvolatile semiconductor memory device according to claim 13, wherein the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation.

15. A nonvolatile semiconductor memory device comprising:
a plurality of sector units, each sector unit comprising a common bulk region, and
wherein each sector unit is configured to be electrically erasable in response to an erase
signal; and
a plurality of memory cell transistors and transistors of a column decoder arranged in
the common bulk region of each sector unit and configured to commonly receive a bulk
voltage.

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16. A nonvolatile semiconductor memory device according to claim 15, wherein
each sector unit further comprises a bulk driver configured to supply a bulk voltage to the
common bulk region.

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17. A nonvolatile semiconductor memory device according to claim 15, wherein
said plurality of memory cell transistors are arranged in a cell array block, wherein said
plurality of column decoder transistors are arranged in a column decoder block, and wherein
said cell array block and said column decoder block are both arranged on the common bulk
region.

18. A method of forming a bulk region of a nonvolatile semiconductor device,
said method comprising:
forming a bulk region for memory cell transistors provided in a cell array block of the
nonvolatile semiconductor memory device; and
forming a bulk region for decoder transistors of a column decoder in the bulk region
for the memory cell transistors of the cell array block.

19. A method of forming a bulk region of a nonvolatile semiconductor device,
according to claim 18, further comprising configuring the bulk regions for the memory cell
transistors and decoder transistors to receive a common bulk signal during an erase operation.

20. A method of forming a bulk region of a nonvolatile semiconductor device,
according to claim 18, wherein said memory cell transistors and said decoder transistors are
configured to be simultaneously erased with each other during an erase operation.

21. (New) A nonvolatile semiconductor memory device comprising:

21 a plurality of sectors, wherein each sector further comprises a plurality of memory cell transistors arranged in a (M x N) array having M word lines and N bit lines where M is at least equal to two; wherein each sector further comprises N decoder transistors corresponding to one of the N bit lines, wherein the plurality of memory cell transistors and the N decoder transistors share a common bulk region, and wherein the semiconductor memory device is configured to electrically erase the plurality of memory cell transistors simultaneously.

22. (New) A sector structure of a nonvolatile semiconductor memory, the sector structure comprising:

22 a plurality of memory cell transistors arranged in a (M x N) array where M is at least equal to two; and

22 N decoder transistors, wherein the plurality of memory cell transistors and the N decoder transistors are arranged on a common bulk region.

23. (New) A nonvolatile semiconductor memory device, comprising:

23 a (M x N) array, wherein M is at least equal to two, comprising a plurality of memory cell transistors having gates and drains, each gate connected to a corresponding one of M word lines, each drain connected to a corresponding one of N bit lines;

23 a source line driver commonly connected to a source of each of the plurality of memory cell transistors;

23 a column decoder comprising N column decoder transistors connected between the N bit lines and a common data line;

23 a common bulk region, wherein the plurality of memory cell transistors and the N column decoder transistors share the common bulk region; and

23 a bulk driver configured to commonly apply a bulk voltage to the common bulk region.

24. (New) A nonvolatile semiconductor memory device comprising:

24 a plurality of sector units, each sector unit comprising a common bulk region wherein each sector unit is configured to be electrically erasable in response to an erase signal, wherein each of the plurality of sector units further comprises a (M x N) array of memory cell transistors arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage, wherein M is at least equal to two, and wherein each of the

plurality of sector units further comprises a (1 x N) array of column decoder transistors arranged in the common bulk region of each sector unit and configured to commonly receive the bulk voltage.

25. (New) A method of forming a bulk region of a nonvolatile semiconductor device comprising:

forming a first bulk region for a plurality of memory cell transistors provided in a (M x N) array, wherein M is at least equal to two; and

forming a second bulk region for N column decoder transistors, wherein the first and the second bulk regions are integrally connected.